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Notice of Allowability	Application No.	Applicant(s)	
	10/717,737	ZHU ET AL.	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Applicants' amendment filed February 21, 2006*.

2. ☒ The allowed claim(s) is/are *2,3,5-13,16,18-25 and 48-58*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Ida M. Soward
AU 2822

DETAILED ACTION

This Office Action is in response to the Applicants' amendment filed February 21, 2006.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Charles W. Peterson, Jr. on May 9, 2006.

The application has been amended as follows:

Claim 48. (currently amended) A field effect transistor (FET) comprising:

a fin formed on a dielectric surface;

a device gate along one side of said fin;

a back bias gate along all opposite side of said fin;

a device gate dielectric along one first side between said device gate and said fin; and

a back bias gate dielectric along said opposite side between said back bias gate and said fin, wherein said back bias gate dielectric differs from said device gate dielectric in material, wherein one of said device gate dielectric and

said back bias gate dielectric ~~are~~ **is** a layered dielectric comprising at least 2 dielectric material layers.

Claim 50. (currently amended) An integrated circuit (IC) on a semiconductor on insulator (SOI) chip, said IC including a plurality of field effect transistors (FETs) disposed on an insulating layer, each of said FETS comprising:

a semiconductor fm formed on an insulating layer;

a device gate dielectric along a first side of said semiconductor fin;

a device gate along said device gale dielectric;

a back bias gate dielectric along an opposite side of said semiconductor fin;

a back bias gate along said back bias gate dielectric, wherein said back bias gate dielectric differs from said device gate dielectric in material, wherein one of said device gate dielectric and said back bias gate dielectric ~~are~~ **is** a layered dielectric comprising at least 2 dielectric material layers.

Allowable Subject Matter

Claims 2-3, 5-13, 16, 18-25 and 48-58 are allowed.

The following is an examiner's statement of reasons for allowance: The prior art of record does not disclose, make obvious, or otherwise suggest the structure of the applicant's together with the other limitations of the independent claims, such as:

in regard to claims 48 and 50, "wherein said back bias gate dielectric differs from said device gate dielectric in material, wherein one of said device gate dielectric and

said back bias gate dielectric are a layered dielectric comprising at least 2 dielectric material layers"; and

in regard to claim 49, "wherein said back bias gate dielectric is five times (5X) thicker than said device gate dielectric". The dependent claims being further limiting and definite are also allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to dual gate FinFETs:

Chang et al. (US 6,291,855 B1)

Chen et al. (US 6,504,207 B1)

Doris et al. (US 6,911,383 B2)

Fan et al. (US 6,747,310 B2)

Forbes (US 2004/0174734 A10

Hisamune (5,929,480)

Kelley et al. (US 6,313,500 B1)

Liang et al. (US 6,281,545 B1)

Mathew et al. (US 6,903,967 B2)

Mathew et al. (US 6,831,310 B1)

Shone et al. (US 6,268,622 B1)

Takamura (US 6,809,374 B2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
May 9, 2006

Ida M. Soward
AU 2822